REMARKS

Claims 1-10 and 19-30 are pending in this application, of which claims 1, 19, 20, 21 and 30 have been amended. No new claims have been added.

Claims 1, 2, 7, 19, 26 and 30 stand rejected under 35 USC §102(e) as being anticipated by either U.S. Patent 6,265,778 to Tottori (hereinafter " **Tottori**") or U.S. Patent No. 6,078,088 to Buynoski (hereinafter "**Buynoski**").

Applicant respectfully traverses this rejection.

Tottori discloses a semiconductor device with a multi-level interconnection structure having a first conductive layer disposed below a fuse, and formed in the same layer as the first metal wire as a component of multi-level interconnects, and a second conductive layer disposed below the fuse and formed in the same layer as the second metal wire as a component of the multi-level interconnects.

The Examiner has identified partitioned intermediate metal layers 22, 32, 22.

Buynoski discloses a low dielectric semiconductor device with a rigid lined interconnection system.

The Examiner has identified intermediate metal 2 having partitioned layers.

The first conductive layer in **Tottori** is not connected to a VIA and is provided for absorbing light not absorbed with laser beam irradiated on a fuse 31.

On the other hand, in the present invention, an intermediate metal layer wiring area not to be connected to a VIA is provided for wiring a signal line, a power source, and the like, which is not disclosed in either of the cited references.

Thus, **Tottori** cannot provide the enhanced degree of wiring flexibility provided in the present invention.

Thus, the 35 USC §102(e) rejections should be withdrawn.

Claims 20 and 21 stand rejected under 35 USC §102(e) as anticipated by or, in the alternative, under USC §103(a) as unpatentable over **Tottori** or **Buynoski**.

Applicant respectfully traverses this rejection.

As noted above, neither of these cited references teaches, mentions or suggests an intermediate metal layer wiring area not connected with the stack VIA but used for wiring, as in the present invention.

Accordingly, claims 20 and 21 have been amended to recite this distinction, and the 35 USC §102(e) rejection should be withdrawn.

Claims 3-6 and 22-25 stand rejected under USC §103(a) as unpatentable over **Tottori** or **Buynoski** taken with U.S. Patent Publication 2003/0006435 to Ono (hereinafter "**Ono**").

Applicant respectfully traverses this rejection.

Ono, **Tottori** and **Buynoski** all fail to disclose the limitations of claims 3-6 and 22-25 relating to a priority wiring direction for forming the intermediate metal layer wiring area because none of these references teaches such a wiring area.

Thus, the 35 USC §103(a) rejection should be withdrawn.

Claims 8-10 and 27-29 stand rejected under USC §103(a) as unpatentable over **Tottori** or **Buynoski**.

As noted above, neither of these cited references teaches, mentions or suggests the limitations added to claims 1 and 19, from which these claims depend.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-10 and 19-20, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Petition for Extension of Time

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